CLAIMS

What is claimed is:

1. A gated diode memory cell comprising:

at least one transistor; and

a gated diode in signal communication with the at least one transistor.

2. A gated diode memory cell as defined in Claim 1 wherein a first terminal of the gated diode forms one terminal of a storage cell and a second terminal of the gated diode forms another terminal of the storage cell.

3. A gated diode memory cell as defined in Claim 2 wherein the gate of the gated diode is implemented in the form of a shallow trench.

4. A gated diode memory cell as defined in Claim 3, the gate of the gated diode comprising a poly trench surrounded by thin oxide with silicon disposed underneath and surrounding the thin oxide.

5. A gated diode memory cell as defined in Claim 4 wherein the poly trench is cylindrical.

6. A gated diode memory cell as defined in Claim 4, the gate of the gated diode comprising a metal oxide semiconductor ("MOS") capacitor.

7. A gated diode memory cell as defined in Claim 2 wherein the gate of the gated diode is planar.

8. A gated diode memory cell as defined in Claim 7 wherein the gate of the gated diode is disposed above a diffusion area.

9. A gated diode memory cell as defined in Claim 8, further comprising an oxide layer disposed between the gate of the gated diode and the diffusion area.

10. A gated diode memory cell as defined in Claim 7, the gated diode comprising a planar metal oxide semiconductor ("MOS") capacitor.

11. A gated diode memory cell as defined in Claim 1 wherein:

the at least one transistor is a field effect transistor ("FET"); and

the gate of the gated diode is in signal communication with the source of the FET.

12. A gated diode memory cell as defined in Claim 11, further comprising a metal connector in signal communication between the source of the field effect transistor and the gate of the gated diode.

13. A gated diode memory cell as defined in Claim 12 wherein the metal connector is a direct metal connector ("MCBAR").

14. A gated diode memory cell as defined in Claim 11 wherein:

the gate of the gated diode forms one terminal of the storage cell; and

at least one of the source of the gated diode forms another terminal of the storage cell.

15. A gated diode memory cell as defined in Claim 14 wherein:

the drain of the FET is in signal communication with a bitline ("BL"); and

the gate of the FET is in signal communication with a write wordline ("WLw").

16. A gated diode memory cell as defined in Claim 15 wherein at least one of the source of the gated diode is in signal communication with a read wordline ("WLr").

17. A gated diode memory cell as defined in Claim 1 wherein:

the at least one transistor comprises first and second FETs with the source terminal of the first in signal communication with the gate terminal of the second; and

the gate terminal of the gated diode is in signal communication with the source terminal of the first FET.

18. A gated diode memory cell as defined in Claim 17 wherein:

the at least one transistor is a field effect transistor ("FET"); and

the gate of the gated diode is in signal communication with the source of the FET.

19. A gated diode memory cell as defined in Claim 18 wherein:

the gate of the gated diode forms one terminal of the storage cell; and

at least one of the source of the gated diode forms another terminal of the storage cell.

20. A gated diode memory cell as defined in Claim 19 wherein:

the drain of the FET is in signal communication with a bitline ("BL"); and

the gate of the FET is in signal communication with a write wordline ("WLw").

21. A gated diode memory cell as defined in Claim 20 wherein the bitline is a combined bitline in signal communication with a drain of an another FET in a single read/write configuration.

22. A gated diode memory cell as defined in Claim 20 wherein the bitline is a separated bitline in a dual read/write configuration.

23. A gated diode memory cell as defined in Claim 17 wherein:

the gate of the gated diode forms one terminal of the storage cell and at least one of the source of the gated diode forms another terminal of the storage cell.

24. A gated diode memory cell as defined in Claim 23 wherein:

the drain of the first FET is in signal communication with a bitline ("BL"); and

the gate of the first FET is in signal communication with a write wordline ("WLw").

25. A gated diode memory cell as defined in Claim 23 wherein at least one of the source of the gated diode is in signal communication with a read wordline ("WLr").

26. A gated diode memory cell as defined in Claim 1 wherein the gated diode comprises an FET.

27. A gated diode memory cell as defined in Claim 26 wherein the drain of the implementing FET for the gated diode is left open.

28. A gated diode memory cell as defined in Claim 26 wherein the source of the implementing FET for the gated diode is left open, and the drain of the implementing FET for the gated diode becomes the source of the gated diode.

29. A gated diode memory cell as defined in Claim 26 wherein the drain of the implementing FET for the gated diode is connected to the source of the implementing FET for gated diode.

30. A gated diode memory cell as defined in Claim 1 wherein the gated diode comprises at least one "partial" FET.

31. A gated diode memory cell as defined in Claim 30 wherein the drain of the gated diode FET is left open to form one "partial" FET with the gate and source.

32. A gated diode memory cell as defined in Claim 30 wherein the source of the gated diode FET is left open to form one "partial" FET with the gate and drain, and the drain of the gate diode FET becomes the source of the gated diode.

33. A gated diode memory cell as defined in Claim 30 wherein the drain of the gated diode FET is connected to the source of the gated diode FET to form two "partial" FETs in parallel.

34. A gated diode memory cell comprising:

at least one switching means; and

directional means in signal communication with the at least one switching means.

35. A gated diode memory cell as defined in Claim 34 wherein a first terminal of the directional means is in signal communication with a first terminal of the switching means.

36. A gated diode memory cell as defined in Claim 35 wherein:

the first terminal of the directional means forms one terminal of the storage cell; and

a second terminal of the directional means forms another terminal of the memory cell.

37. A gated diode memory cell as defined in Claim 36 wherein:

a second terminal of the switching means is in signal communication with a bitline ("BL"); and

a third terminal of the switching means is in signal communication with a write wordline ("WLw").

38. A gated diode memory cell as defined in Claim 36 wherein the second terminal of the directional means is in signal communication with a read wordline ("WLr").

39. A gated diode memory cell as defined in Claim 34 wherein:

the at least one switching means comprises first and second switching means with the first terminal of the first in signal communication with a third terminal of the second; and

the first terminal of the directional means is in signal communication with the first terminal of the first switching means.

40. A gated diode memory cell as defined in Claim 39 wherein:

the first terminal of the directional means forms one terminal of the memory cell and the second terminal of the directional means forms another terminal of the memory cell.

41. A gated diode memory cell as defined in Claim 40 wherein:

the second terminal of the first switching means is in signal communication with a bitline ("BL"); and

the third terminal of the first switching means is in signal communication with a write wordline ("WLw").

42. A gated diode memory cell as defined in Claim 41 wherein the second terminal of the directional means is in signal communication with a read wordline ("WLr").

43. A gated diode memory cell as defined in Claim 42 wherein a third terminal of the directional means is left open.

44. A gated diode memory cell as defined in Claim 42 wherein a third terminal of the directional means is connected to the second terminal of the directional means.

45. A gated diode memory cell as defined in Claim 34, further comprising:

1-data writing means for writing a 1-data to the memory cell with the gate of the gated diode at a High voltage by storing a charge corresponding to the 1-data in the inversion layer between the gate and a channel; and

0-data writing means for writing a 0-data to the memory cell with the gate of the gated diode at a Low or Zero voltage by storing substantially no charge corresponding to the 0-data in the inversion layer between the gate and a channel.

46. A gated diode memory cell as defined in Claim 45 wherein the memory cell voltage has a voltage gain during a Read operation.

47. A memory array comprising a plurality of gated diode memory cells, each of the plurality of gated diode memory cells as defined in Claim 1.

48. A memory array as defined in Claim 47, the array comprising a plurality of rows and a plurality of columns of gated diode memory cells.

49. A memory array as defined in Claim 47 wherein the plurality of gated diode memory cells comprises 2T1D memory cells arranged in rows, each 2T1D memory cell of at least part of a row sharing a common Read Device GND.

50. A memory array as defined in Claim 47 wherein the source terminal of the at least one transistor can be biased at a voltage.

51. A memory array as defined in Claim 49 wherein each 2T1D memory cell of at least part of a row shares a common biasing voltage line.

52. A method of writing to a gated diode memory cell where the source of the gated diode is at a Low voltage, the method comprising at least one of:

writing a 1-data to the memory cell with the gate of the gated diode at a High voltage by storing a charge corresponding to the 1-data in the inversion layer between the gate and a channel; and

writing a 0-data to the memory cell with the gate of the gated diode at a Low or Zero voltage by storing substantially no charge corresponding to the 0-data in the inversion layer between the gate and a channel.

53. A method as defined in Claim 52 wherein the memory cell voltage has a voltage gain during a Read operation.